REMARKS

Applicants respectfully request the Examiner's reconsideration of the present application as amended.

Claims 15-17, 23-42, 44-69, 72 and 73 are pending in the present application.

Claims 15-17 and 23-25 are allowed.

Claims 33 and 38 are objected to because of informalities.

Claims 68-69 are objected to under 35 U.S.C. §112, second paragraph.

Claims 26-29, 34, 39-42, 44, 46-47, 53-62, 65, 68-69, and 72-73 are rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent 5,659,484 ("Bennett").

Claims 30-33, 35-38, 63-64, 66-67 are rejected under 35 U.S.C. §103(a) as being unpatentable over Bennett in view of U.S. Patent 5,521,837 ("Frankle").

Claims 45, and 48-52 are rejected under 35 U.S.C. §103(a) as being unpatentable over Bennett in view of U.S. Patent 5,541,849 ("Rostoker").

Claims 68-69 have been canceled.

Claims 33 and 38 have been amended to correct a typo.

Support for the amended claims is found on pages 4-28 of the specification, Figures 1-8(k) of the drawings, and claims 1-71 as originally filed. No new matter has been added.

Claims 33 and 38 are objected to because of informalities.

Claims 33 and 38 have been amended according to the suggestions provided by the Examiner.

Applicants submit that in view of the amendment to claims 33 and 38, the objections to claims 33 and 38 have been overcome.

Claims 68-69 are objected to under 35 U.S.C. §112, second paragraph.

Claims 68-69 have been canceled.

Claims 26-42, 44-67, and 72-73 are rejected claims under 35 U.S.C. §102(b) and §103(a) as being unpatentable over Bennett, Frankle, and Rostoker. In particular, the Office Action mailed 8/24/2006 states that

> Although Bennett et al. teaches the minimum and maximum delay budgets (mintarget and maxtarget) are independently calculated as pointed out by Applicant, such calculations of the minimum/maximum delay budgets are based on at least some common variables (i.e., sumdelay, path.numconns, conn.delay being used for both the mintarget and maxtarget – col. 19, lines 30-60) and the both the conn.mindelta and conn.maxdelta (components of the calculation of the minimum/maximum delay budgets min target and maxtarget respectively) must be zero to end the recursive timing budget relaxation (see col. 20, lines 59-67). Therefore, the minimum and maximum delay budgets are accordingly computed at least indirectly and/or directly in consideration of each other.

(8/24/2006 Office Action, p. 11).

It is submitted that Bennett, Frankle, and Rostoker do not render claims 15-17, and 26-42, 44-67, and 72-73 unpatentable under 35 U.S.C. §102(b) and §103(a).

Bennett includes a disclosure of a device independent, frequency driven layout system and method for field programmable gate arrays ("FPGA") which allow for a circuit designer to specify the desired operating frequencies of clock signals in a given design to the automatic layout system to generate, if possible, a physical FPGA layout which will allow the targeted FPGA device to operate at the specified frequencies. Actual net, path and skew requirements are automatically generated and fed to the place and route tools. The system and method disclosed evaluates the frequency constraints, determines what delay ranges are acceptable for each electrical connection and targets those ranges throughout the layout. (see Bennett Abstract).

Frankle includes a disclosure of suggested delay limits for use by layout tools which cause a programmable integrated circuit device to implement a logic design. The suggested delay limits can be used by such tools as an initial placement algorithm, a placement improvement algorithm, and a routing algorithm for evaluating and guiding potential layouts. The suggested delay limits take into account characteristics of the programmable device being used by

estimating lower bound delays for each connection in a logic design, and take into account any previously achieved delays or achievable delays for each connection in calculating the suggested limits. Results of routing benchmark designs using the novel suggested limits show improved timing performance for all benchmark cases tested. (see Frankle Abstract).

Rostoker includes a disclosure of a methodology for generating structural descriptions of complex digital devices from high-level descriptions and specifications. The methodology uses a systematic technique to map and enforce consistency of the semantics imbedded in the intent of the original, high-level descriptions. The design activity is essentially a series of transformations operating upon various levels of design representations. At each level, the intended meaning (semantics) and formal software manipulations are captured to derive a more detailed level describing hardware meeting the design goals. Features of the methodology include: capturing the users concepts, intent, specification, descriptions, constraints and trade-offs; architectural partitioning; what-if analysis at a high level; sizing estimation; timing estimation; architectural trade-off; conceptual design with implementation estimation; and timing closure. The methodology includes using estimators, based on data gathered over a number of realized designs, for partitioning and evaluating a design prior to logic synthesis. From the structural description, a physical implementation of the device is readily realized. Techniques are provided for estimating design performance, from behavioral/functional descriptions. Given a behavioral or a block diagram description of data flow in a design, pin-to-pin timing and minimum clock cycle for the design can be estimated accurately. An RTL description may thus be synthesized from a behavioral description such that timing constraints imposed at the behavioral level are achieved. The timing of a synthesized design is estimated, and the design is re-synthesized until a design is arrived at that meets timing constraints imposed at a higher level. (See Rostoker Abstract).

It is submitted that Bennett, Frankle, and Rostoker do not teach or suggest generating minimum and maximum delay budgets for connections from long-path and short-path timing

constraints, wherein for each connection the minimum and maximum delay budgets are determined such that at least one of the minimum delay budgets and maximum delay budgets is determined with consideration of the other.

On the contrary, Bennett discloses computation of minimum delay targets (mintarget/con.mintarget) and maximum delay targets (maxtarget/conn.maxtarget) that are computed independently of each other. Bennett provides a pseudocode representation of the Compute Connection Target process used (col. 19, lines 31-61). The pseudocode illustrates that maxtarget is computed from the values maxslack, path.numconns, conn.delay, and sumdelay. The pseudocode illustrates that mintarget is computed from the values minslack, path.numconns, conn.delay, sumdelay (col. 19, lines 44-47, lines 49-54, lines 56-61). The variables maxtarget and mintarget are computed independently and without consideration of each other.

The Office Action mailed 8/24/2006 acknowledges that the mintarget and maxtarget are independently calculated, but states that such calculation "are based on at least some common variables (i.e., sumdelay, path.numconns, conn.delay being used for both the min target and maxtarget – col. 19, lines 30-60) ... Therefore, the minimum and maximum delay budgets are accordingly computed at least indirectly and/or directly in consideration of each other." (8/24/2006 Office Action, p. 11).

Applicants respectfully disagree. Claims 26 and 59 include the limitation that "at least one of the minimum delay budgets and maximum delay budgets is determined with consideration of the other". This requires either 1) the minimum delay budget is determine with consideration of the maximum delay budget, or 2) the maximum delay budget is determined with consideration of the minimum delay budget. Although the mintarget and maxtarget disclosed in Bennett are computed using some common variables, this is not equivalent to having mintarget determined with consideration of maxtarget or having maxtarget determined with consideration of mintarget. There are one or more variables required for computing mintarget, such as minslack, that are not used for computing maxtarget. Furthermore, there are one or more variables required for

computing maxtarget, such as maxslack, that are not used for computing mintarget. Applicants submit that in order for mintarget to be determined with consideration of the maxtarget, either all variables and parameters associated with maxtarget, including maxslack, or the maxtarget values themselves must be considered. Furthermore, in order for maxtarget to be determined with consideration of the mintarget, either all variables and parameters associated with mintarget, including minslack, or the mintarget values themselves must be considered. This is not the case in Bennett.

Applicants present the following examples to illustrate that Bennett discloses a procedure where 1) the maxtarget may change without affecting the mintarget, and 2) the mintarget may change without affecting the maxtarget, thus further illustrating that the procedure in Bennett does not compute minimum delay budgets and maximum delay budgets that are determined with consideration of the other.

Given a single connection between A and B.
A -> B

This connection forms a single path.
A -> B

The connection delay (conn.delay) of A->B is 2, and that the sumdelay = conn.delay since this is a single-connection path.

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long-path requirement: 4
short-path requirement: 2

minslack(short-path requirement = 2, conn.delay = 2) = 0
maxslack(long-path requirement = 4, conn.delay = 2) = 2

mintarget = conn.delay - (conn.delay / sumdelay) * minslack
= 2 - (2 / 2) * 0 = *2*
maxtarget = conn.delay + (conn.delay / sumdelay) * maxslack
= 2 + (2 / 2) * 2 = *4*

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long-path requirement: -100
short-path requirement: 2

minslack(short-path requirement = 2, conn.delay = 2) = 0
maxslack(long-path requirement = -100, conn.delay = 2) = -102

mintarget = conn.delay - (conn.delay / sumdelay) * minslack
= 2 - (2 / 2) * 0 = ***2***
maxtarget = conn.delay + (conn.delay / sumdelay) * maxslack
= 2 + (2 / 2) * (-102) = ***-100***

Note that by using the procedure disclosed in Bennett, changing the long-path requirement affects the maxslack and the maxtarget without affecting the mintarget. Clearly, mintarget (held constant at 2) is not determined in consideration of maxtarget which changes from 4 to -100.

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long-path requirement: 4
short-path requirement: 100

minslack(short-path requirement = 100, conn.delay = 2) = -98
maxslack(long-path requirement = 4, conn.delay = 2) = 2

mintarget = conn.delay - (conn.delay / sumdelay) * minslack
= 2 - (2 / 2) * (-98) = ***100***
maxtarget = conn.delay + (conn.delay / sumdelay) * maxslack
= 2 + (2 / 2) * 2 = ***4***

Note that by using the procedure disclosed in Bennett, changing the short-path requirement affects the minslack and the mintarget, without affecting the maxtarget. Clearly, maxtarget (held constant at 4) is not determined in consideration of mintarget which changes from 2 to 100.

Thus, because the procedure in Bennett computes mintargets and maxtargets independently of each other, neither the mintargets nor the maxtargets are determined with consideration of the other.

Frankle only discloses a timing driven method for laying out a user's circuit onto a programmable integrated circuit device.

Rostoker only discloses a method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including estimation and comparison of timing parameters.

In contrast, amended claim 26 states

> A method for designing a system, comprising:
> generating minimum and maximum delay budgets for connections from long-path and short-path timing constraints, wherein for each connection the minimum and maximum delay budgets are determined such that at least one of the minimum delay budgets and maximum delay budgets is determined with consideration of the other; and
> designing the system in response to the minimum and maximum delay budgets.

(Claim 26, as Amended) (Emphasis added).

Claim 59 includes similar limitations. Given that claims 27-42, 44-58, and 72-73 depend directly or indirectly from claim 26 and claims 60-67 depend directly or indirectly from claim 59, it is likewise submitted that claims 27-42, 44-58, 72-73, and 60-69 are also patentable under 35 U.S.C. §102(b) and §103(a) over Bennett, Frankle, and Rostoker.

Applicants submit that amended claims 26-42, 44-67, and 72-73 are patentable under 35 U.S.C. §102(b) and §103(a) over Bennett, Frankle, and Rostoker.

In view of the amendments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 15-17, 23-42, 44-67, and 72-73 should be found to be in condition for allowance.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

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Lm. Cl

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